EXHIBIT T

Exhibit 12 – Sudha et al.

'156 Patent

Claim Limitation (Claim 7)	Exemplary Disclosure
[**156a**] A device comprising:	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses a device. *See, e.g.,*: "Principal Component Analysis (PCA) finds wide applications in machine vision. The neural network that performs PCA Is called Principal Component Neural Network (PCNN). This paper presents a digital hardware design for principal component neural network. The design is efficient in the sense that the learning rule is implemented with a reusable circuit. Results of FPGA implementation of the design show that as many as 500 input vectors can be processed during training phase and 700 input vectors during retrieval phase in a second. Such results are valuable for high-speed applications." Sudha et al., *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, at 1.
[**156b**] at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See, e.g.,*: "The hardware design of a 64-input 16-output PCNN was coded in Verilog hardware description language. Each parameter in the design is represented as a floating point number with an 8-bit mantissa and an 8-bit exponent." Sudha et al., *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, at 428. "The details of each computational unit in the arithmetic unit that implements an *N*-input *M*-output PCNN are given below. Each data element is represented as a floating point number with *p*-bit exponent in twos-complement form." *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, at 427. "The slice of the Virtex device contains two logic cells, which realizes the combinational logic of the design. Two such slices comprise one configurable logic block (CLB). The input/output

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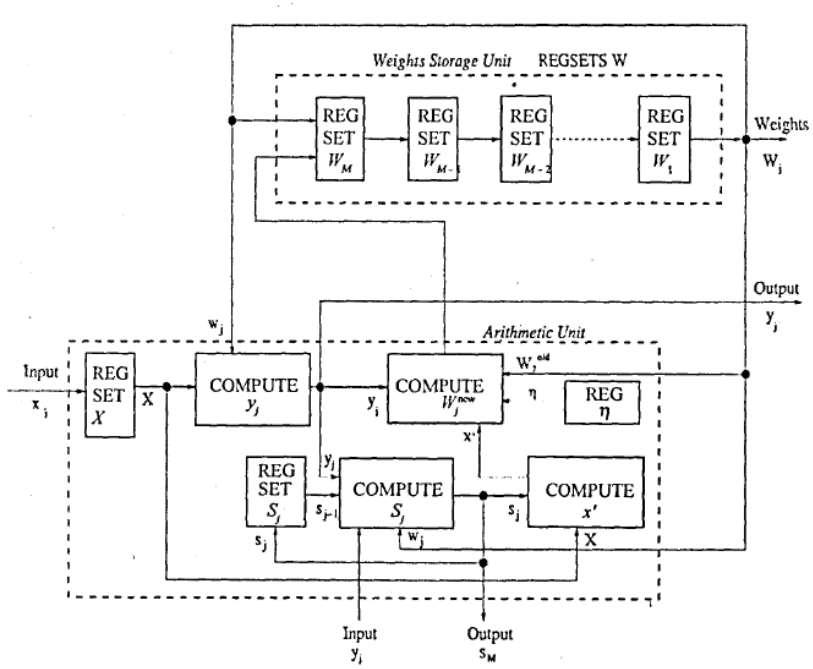
	blocks (lOBs) provide the interface between the device pins and the CLBs. The device has 1 million gates." Sudha et al., *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, at 429. *See also* Sudha et al., *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, at 427, Fig. 2 (depicting input and output).  Fig 2 Block diagram of hardware design for PCNN.
[**156c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over

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1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input; and	repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See, e.g.,*: "The hardware design of a 64-input 16-output PCNN was coded in Verilog hardware description language. Each parameter in the design is represented as a floating point number with an 8-bit mantissa and an 8-bit exponent. The functional behaviour of the design was tested in ModelSim (a package for functional simulation of VLSI design). The principal components were extracted from a given data set by the GHA algorithm implemented in Matlab. The components computed by the hardware algorithm for the same data set were compared with them for correctness." Sudha et al., *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, at 428. *See* Appendix to Responsive Contentions Regarding Non-Infringement and Invalidity (detailing error rates associated with different mantissa sizes, including 8-bit mantissa and 8-bit exponents).
[**156d**] at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit;	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit. *See, e.g.,*: "Principal Component Analysis (PCA) finds wide applications in machine vision. The neural network that performs PCA Is called Principal Component Neural Network (PCNN). This paper presents a digital hardware design for principal component neural network. The design is efficient in the sense that the learning rule is implemented with a reusable circuit. Results of FPGA implementation of the design show that as many as 500 input vectors can be processed during training phase and 700 input vectors during retrieval phase in a second. Such results are valuable for high-speed applications." Sudha et al., *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, at 425.

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Claim Limitation (Claim 7)	Exemplary Disclosure
	"A systolic array mapping of Adaptive Principal Component Extraction (APEX) is discussed in [5]. An n-input m-output PCNN can be mapped to an array of m processing elements (PEs). Separate phases. Each PE has memory to store synaptic weights, arithmetic and local control units. It takes $n + 2m - 1$ time units to complete the updating of weights for one input pattern during the training phase and m time units are required between successive input patterns during retrieval phase." Sudha et al., *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, at 425-26. To the extent that Singular contends that Sudha et al. do not identify a device adapted to the control the operation of at least one first LPHDR execution unit, such a device would have been obvious given the existence of similar devices and intervening developments in device infrastructure for the reasons explained in the Responsive Contentions Regarding Non-Infringement and Invalidity.
[**156e**] wherein the at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine;	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses at least one first computing device comprises at least one of a central processing unit (CPU), a graphics processing unit (GPU), a field programmable gate array (FPGA), a microcode-based processor, a hardware sequencer, and a state machine. *See, e.g.,*: "A systolic array mapping of Adaptive Principal Component Extraction (APEX) is discussed in [5]. An n-input m-output PCNN can be mapped to an array of m processing elements (PEs). Separate phases. Each PE has memory to store synaptic weights, arithmetic and local control units. It takes $n + 2m - 1$ time units to complete the updating of weights for one input pattern during the training phase and m time units are required between successive input patterns during retrieval phase." Sudha et al., *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, at 425-26. "Principal Component Analysis (PCA) finds wide applications in machine vision. The neural network that performs PCA Is called Principal Component Neural Network (PCNN). This paper presents a digital hardware design for principal component neural network. The design is

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Claim Limitation (Claim 7)	Exemplary Disclosure
	efficient in the sense that the learning rule is implemented with a reusable circuit. Results of FPGA implementation of the design show that as many as 500 input vectors can be processed during training phase and 700 input vectors during retrieval phase in a second. Such results are valuable for high-speed applications." Sudha et al., *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, at 428.
[**156f**] and, wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, teaches or suggests that the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide. *See, e.g.,*: "A systolic array mapping of Adaptive Principal Component Extraction (APEX) is discussed in [5]. An n-input m-output PCNN can be mapped to an array of m processing elements (PEs). Separate phases. Each PE has memory to store synaptic weights, arithmetic and local control units. It takes $n + 2m - 1$ time units to complete the updating of weights for one input pattern during the training phase and m time units are required between successive input patterns during retrieval phase." Sudha et al., *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, at 425-26. "The design was mapped on to one of the target devices of Xilinx FPGA using Leonardo Spectrum design tool. The specifications of the chosen target device are as follows: family - VIRTEX; device XCVlOOOBG560. The floorplan of the device for the design is shown in Fig 5. The portions of the FPGA device used for implementing the design can be seen in the figure. Further, the interconnections between the components of the device utilized for the design can be seen. The device utilization is summarized in Table 1. The slice of the Virtex device contains two logic cells, which realizes the combinational logic of the design. Two such slices comprise one configurable logic block (CLB). The input/output blocks (lOBs) provide the interface between the device pins and the CLBs. The device has 1 million gates." Sudha et al., *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, at 425-26.

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Claim Limitation (Claim 7)	Exemplary Disclosure
	For the reasons explained in the Responsive Contentions Regarding Non-Infringement and Invalidity, one of skill in the art applying these teachings of Sudha et al. would have found it obvious to implement ever greater numbers of LPHDR execution units given intervening developments in FPGA technology and manufacturing.

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Claim Limitation (Claim 53)	Exemplary Disclosure
[**273a**] A device:	Sudha et al.’s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses a device. *See* [**156a**].
[**273b**] comprising at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	Sudha et al.’s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].
[**273c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X % of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input;	Sudha et al.’s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**].
[**273d**] wherein the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide.	Sudha et al.’s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, teaches or suggests that the number of LPHDR execution units in the device exceeds by at least one hundred the non-negative integer number of execution units in the device adapted to execute at least the operation of multiplication on floating point numbers that are at least 32 bits wide. *See* [**156f**].

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Claim Limitation (Claim 4)	Exemplary Disclosure
[**961a**] A device comprising:	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses a device. *See* [**156a**].
[**961b**] at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].
[**961c**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input; and	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**].
[**961d**] at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit.	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit. *See* [**156d**].

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Claim Limitation (Claim 13)	Exemplary Disclosure
[**961e**] A device comprising:	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses a device. *See* [**156a**].
[**961f**] a plurality of components comprising:	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**]. Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses at least one first computing device adapted to control the operation of the at least one first LPHDR execution unit. *See* **[156d]**.
[**961g**] at least one first low precision high-dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value,	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses at least one first low precision high dynamic range (LPHDR) execution unit adapted to execute a first operation on a first input signal representing a first numerical value to produce a first output signal representing a second numerical value. *See* [**156b**].
[**961h**] wherein the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=10% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.2% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input.	Sudha et al.'s article, *An Efficient Digital Architecture for Principal Component Neural Network and its FPGA Implementation*, discloses the dynamic range of the possible valid inputs to the first operation is at least as wide as from 1/1,000,000 through 1,000,000 and for at least X=5% of the possible valid inputs to the first operation, the statistical mean, over repeated execution of the first operation on each specific input from the at least X% of the possible valid inputs to the first operation, of the numerical values represented by the first output signal of the LPHDR unit executing the first operation on that input differs by at least Y=0.05% from the result of an exact mathematical calculation of the first operation on the numerical values of that same input. *See* [**156c**].